Customer No.: 31561
Application No.: 10/711,938
Docket No.: 14001-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claim 1, 2, 4-8 and 10 under 35 U.S.C. 102(b) as being anticipated by Gillingham (US-5,903,511, "Gillingham" hereinafter). The Office Action objected claims 3 and 9 as being dependent upon rejected base claims, but would be allowable if rewritten in independent form. Applicants respectfully traverse the rejections addressed to claims 1, 2, 4-8 and 10 for at least the reasons set forth below.

Discussion of Objections

Claims 3 and 9 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form.

Initially, it is noted with great appreciation that the Examiner considers the subject matter of claims 3 and 9 as being allowable over the art of record. In response thereto, the rejection to independent claim 1 has been traversed to make dependent claim 3 allowable. Furthermore, independent claim 7 is also traversed to make dependent claim 9 allowable. In view of the aforementioned, Applicants respectfully assert that the objections are no longer proper.

Discussion of the claim rejection under 35 USC 102

The Office Action has rejected claims 1-2, 4-8, and 10 under 35 U.S.C. 102(b) as being anticipated by Gillingham.

Applicants respectfully traverse the above rejections as set forth below.

The following is disclosed in claim 1 of Gillingham: "**programmable addressing means** for causing the wordlines, once addressed, to selectively enable either one or more than one cell access FET" for a DRAM array. The aforementioned is further supported in Table A in Gillingham, col. 2, lines 8-18. Based on the aforementioned, it is understood that the DRAM array in Gillingham is for a "programmable" version. However, the DRAM array in the present invention does not include the feature of a "programmable addressing means" for "selectively enable either one or more than one cell access FET". As a result, Claims 1, 5, and 7 of the present invention are patentably distinguish over Gillingham in regard to the feature of "programmable" vs. "non-programmable" because Claims 1, 5, and 7 implicitly include the "non-programmable" feature as discussed above.

Furthermore, Gillingham states "...both the program logic signals VppEN=1 and CPB=1 should be used..." in col. 7, lines 56-68 and "Thus when Vpp/EN=0, the pump is disabled, and the Vpp line reverts to the voltage Vdd."in col. 7, lines 35-36. As a result, it is clearly evident that the pump in Gillingham is "programmable" using VppEN. On the other hand, **NO** evidence can be found that the present invention as a whole as well as in Claims 1, 5, and 7 of the present invention discloses any "programmable" functions for the pump described in Gillingham.

Taking another step further, Gillingham indeed uses a charge pump as described in "an input voltage Vdd is **boosted by the pump** to the boosted voltage Vpp, preferably equal to Vdd + Vtn" in col. 5, lines 16-18. On the other hand, the present invention states in paragraph [0029]: "...the maximum voltage is the power voltage VDD provided by the power terminal **without using the charge pump.**" Therefore, unlike in Gillingham, the present invention does not use a charge pump. As a result, although Claims 1 and 7 do not state explicitly of not using the charge pump, Claims 1 and 7 do however implicitly include the fact of not using charge pump through the aforementioned citations from the disclosure of the invention. As a result, this is further evidence that Claims 1 & 7 patentably distinguish over Gillingham.

In addition, Line 12 of Claim 1 in the present invention states: "charging the bit line and the bit line bar to the power voltage;" which is fully supported in paragraph [0026] of the present invention: "According to an embodiment of the present invention, the maximum voltage is the **power voltage VDD provided by the power terminal without using the charge pump. The bit line BL and the bit line bar BLB need not be maintained at the voltages**, such as the transient voltage resulting from sharing the voltage with the memory cell or the transient pull-down voltage, except for the power voltage VDD and the ground voltage GND....." In addition, "The method is capable of operating DRAM **without using a charge pump"** is found in paragraph [0005] of the present invention. On the other hand, Gillingham in col. 7, lines 1-3 states: "In operation, when /VppEN=0, FETs 81 and 82 conduct between Vdd and ground, the output **PRE**

voltage is (Vdd-Vtn)/2, where Vtn is the threshold of conductive of an FET." and in col. 6, line 65 states: "which is the **bitline precharge voltage PRE**".

As a result, the output precharge voltage PRE is clearly defined to be **(Vdd-Vtn)/2** when VppEN=0. Therefore, Claim 1 patentably distinguish over Gillingham based on the fact that the present invention does not require a **(Vdd-Vtn)/2** for precharging as described in Gillingham above when VppEN=0.

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2 and 4 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1.

Furthermore In regards to Claim 5 of the present invention, "wherein the first voltage equals to a voltage obtained by subtracting a switch voltage drop **from a power voltage...**" in Claim 5 of the present invention implicitly contains the same argument presented above for Claim 1 in which the "power voltage VDD provided by the power terminal without using the charge pump". As a result, the "power voltage" in Claim 5 is "without using the charge pump" and is patentably distinguish over Gillingham, which has the output **PRE voltage is (Vdd-Vtn)/2** when VppEN=0 as previously discussed.

If independent claim 5 is allowable over the prior art of record, then its dependent claim 6 is allowable as a matter of law, because the dependent claim 6 contains all features of its respective independent claim 5.

Furthermore in regard to Claim 7, the reading operation of a DRAM includes "charging the bit line and the bit line bar to the power voltage" as found in claim 7 in the present invention. This is fully supported in paragraph [0026] of the present invention:

"According to an embodiment of the present invention, the maximum voltage is the **power voltage VDD provided by the power terminal without using the charge pump. The bit line BL and the bit line bar BLB need not be maintained at the voltages,** such as the transient voltage resulting from sharing the voltage with the memory cell or the transient pull-down voltage, except for the power voltage VDD and the ground voltage GND....." In addition, "The method is capable of operating DRAM **without using a charge pump**" is found in paragraph [0005] of the present invention. On the other hand, Gillingham in col. 7, lines 1-3 states: "In operation, when /VppEN=0, FETs 81 and 82 conduct between Vdd and ground, the output **PRE voltage is (Vdd-Vtn)/2,** where Vtn is the threshold of conductive of an FET." and in col. 6, line 65 states: "which is the **bitline precharge voltage PRE**".

As a result, the output precharge voltage PRE is clearly defined to be **(Vdd-Vtn)/2** when VppEN=0. Therefore, Claim 7 patentably distinguish over Gillingham based on the fact that the present invention does not require a **(Vdd-Vtn)/2** for precharging as described in Gillingham above when VppEN=0.

If independent claim 7 is allowable over the prior art of record, then its dependent claims 8 and 10 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 7.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-10 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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